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Power Minimization by Clock Gating For Low Power in Microprocessor

Shivam Singh Solanki
M Tech Student,
Department of Electronics and Communication Engineering
Takshshila Institute of Engineering & Technology
Jabalpur, (M.P.) India
Email: shivamsolanki.solanki@gmail.com

Prof. Shobhit Verma
Head of the Department
Department of Electronics and Communication Engineering,
Takshshila Institute of Engineering & Technology
Jabalpur, (M.P.) India
Email: shobhitverma@takshshila.org

***Abstract*—**Power consumption has become an important factor in low power VLSI design. The need for power saving design has a large potential. Due to advancement in technology in several years there is a vast need of power sensitive designs. There are many power efficient design techniques have already proposed to reduce power consumption in terms of static and dynamic power dissipation in VLSI architecture. While Scaling the technology for high performance and better functionality, power dissipation has become a major concern for microprocessor designs. Clock power has sufficiently great importance in high performance microprocessor designs. Clock Gating to reduce the prodigal usage of several activities is due indirect addressing in microprocessor efficiently reduces power consumption. Clock gating technique effectively reduces the clock power. In a pipelined stage the usage of a circuit block can be predicted in advance a few timing cycles. Clock Gating uses this advance information to clock gate the circuit blocks which are not used. Depending on different applications, all the circuits are not used at the same time which gives an idea to reduce the clock power significantly. The gate control signal is AND'ed by a clock which incapacitates the clock in a circuit when it is not used, by circumvention power dissipation due to charging and discharging the circuit which are not used. Clock Gating is well planned technique which results in reducing the clock power. By Clock Gating technique 20-35% of power consumption is reduced. In a complex pipelined structures power consumption becomes a serious concern, Clock Gating efficiently helps to reduce power consumption to a vide extent.

1. INTRODUCTION

Low power VLSI design is in demand from recent years its growth has increased significantly. This demand is increasing day by day due to emerging and changing technology of portable battery operated devices such as smart phones, tablets, lab tops and other communication devices. Scaling of these semiconductors has led to the development of high speed and high performance with high integration density. As the density of transistor in a design has increased with increase in high frequency operation, the requirement and consumption of power also increasing in every new technology. The power supply has to be scaled to maintain the consumption of power within the limit. Scaling and reducing the supply voltage or power supply is restricted in high performance devices[1]. Hence by scaling power supply only it is not sufficient to control the power consumption within limit. Circuit and system level abstraction

techniques are required along with previous scaling technique to achieve low power VLSI design. In small signal applications, a large amount of power is consumed in high performance digital circuits because of large amount of leakage current. In small signal applications the leakage power increases power consumption during operation and reduces the availability of power which in turn affects the device performance[1,6]. Therefore some minimization techniques are necessary to improve the device performance while reducing the leakage power. Some low power consumption techniques are required to reduce total leakage in small signal applications such as nano-scale devices. Some techniques for low power

VLSI design such as Merge and Split Clock Gate have already been developed so far.

2.CLOCK GATING TO REDUCE POWER

In digital circuits, it is a powerful technique in reduction of dynamic power dissipation, used extremely in many synchronous circuits. This process called clock gating which prevents more power by adding more logic to circuits to prune the clock tree[8]. If there is no need of switch states in flip flops and pruning of clock is done which disable the portions of circuitry. Normally, in synchronous circuit like the general purpose microprocessor, at a given time only a portion of the circuit is active that's how unwanted power dissipation can be reduced by shutting down the idle portion of the circuit. Best way to carry out this process is the masking of clock which goes to the idle portion of the circuit[2,8,16].

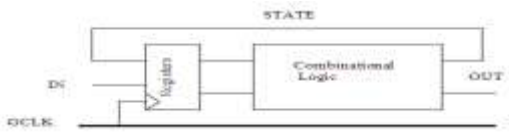

Figure 2.1:Single Clock Flip Flop based FSM

This process helps in reducing unnecessary switching of the inputs to the idle circuit block, which results in reducing the dynamic power. The input is given through registers in combinational logic, which are generally made up of sequential elements, like D flip-flops.

When combinational block is not used and to have binary zero in local clock (***LCLK***), a control signal (***fa***) is used. A gated clock design can be obtained by modifying the clocking structure shown in Fig.11. When ***fa*** is high local clock is blocked. The latch shown in Fig.12 is important to anticipate any glitches in f_a from propagating to the AND gate when the global clock (***GCLK***) is high. The circuit operates as follows.

Before the rising edge of the global clock, the signal ***fa*** is valid only. If ***fa*** is high while low-to-high transition of the global clock, then AND gate will block global clock so local clock will always be low. And at low global clock, we have transparent latch in spite of which, the AND gate is not affected by ***fa***.

Power saving using gated clock technique strongly depends on the optimization of dedicated clock-stopping circuitry and efficient synthesis[2,16].

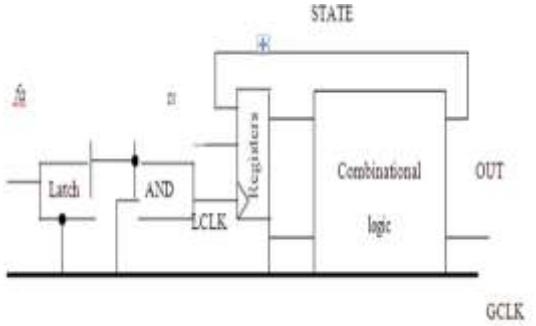

Figure 2.2: Gated Clock Diagram

To know which circuits are gated, when and for how long, a methodology is needed to have effective clock gating. Clock-gating schemes that either apply clock gating to those small blocks so that we get larger clock gating control circuitry as blocks only, incur large overhead or in

between enabled and disabled states, result in frequent toggling of the clock-gated circuit. All this may result into higher power dissipation than that without clock gating.

3. GENERAL PURPOSE MICROPROCESSOR

The particular instructions which is general -purpose microprocessor can execute and the respective encoding are defined in the figure shown above. And the Instruction column shows the mnemonic and syntax to use for the instruction while writing a program in the assembly language. Encoding column represents the instruction's binary encoding and the Operation column represents the instruction's actual operation. The instructions are divided mainly into four types:

1. To transfer data between the accumulator, the general registers and the memory
2. Data movement instructions
3. To change the instruction execution sequence, jump instructions are used.
4. To perform arithmetic and logical, arithmetic and logic instructions are used.
5. There are five data movement instructions, ten arithmetic, logic instructions and eight jump instructions, two input/output instructions, and two miscellaneous instructions in Input / Output and miscellaneous instructions[21].

The number of instructions implemented find outs the number of bits needed to encode the instructions. And all instructions those are encoded with the use of one byte except for instructions which have a memory address as its operand, in this case for address, second byte is needed. The first four bits are used for encoding scheme as the opcode. As dependent on the opcode, the last four bits are interpreted differently like this[21,6].

4. IMPLEMENTATION OF DETERMINISTIC CLOCK GATING

4.1 Execution Units

After every instruction issue, it is known that which execution units will be used in the execute stage prior to some cycles in the future. In an issue queue the selection logic does not selects the instructions which are to be issued based on the availability of execution unit, it also incorporates the instructions in the execution unit. Hence, the selection logic is enhanced and provides the information that which execution units will not be used and clock-gate those respective units.

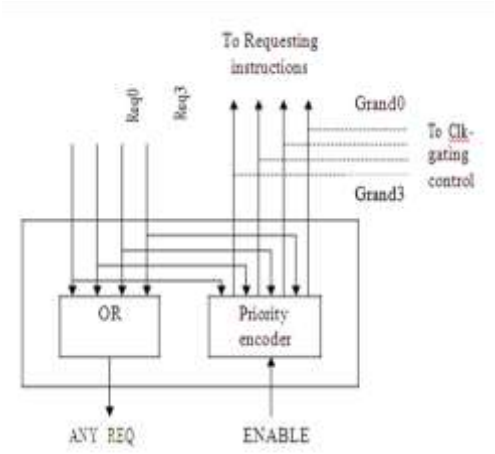

Fig 4.2 Schematic of a selection logic cell with the clock-gate signals extracted from it.

Figure 4.2 depicts the schematic of selection logic incorporated with one type of execution unit (e.g., integer Arithmetic Logic Unit, or floating-point adder or multiplier, etc.). The request signals (REQ) come from the ready instructions after the wakeup logic determines which instructions are ready. The selection logic an scheme to select a subset of the ready instructions, and generates the corresponding grant signals (GRANT) in order to grant it., we The GRANT signals is send to the clock-gate control in our implementation[2,22].

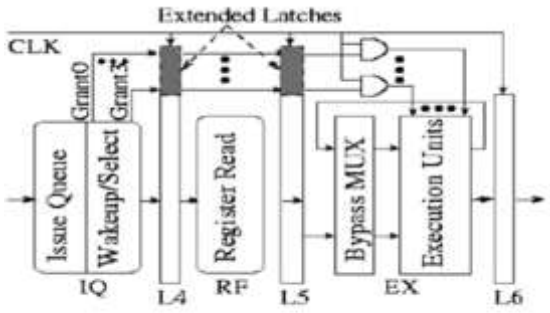

Fig 4.3. Clock-gating of the execution units.

Figure 4.3 shows the control unit in pipeline stage. The instructions which is selected in X cycle uses the execution units in cycle (shown in Figure. 4.4), the GRANT signals is passed down the pipeline through latches to clock gate them in appropriate timing. The pipeline latches for the issue and read stages are extended by some extra bits which holds the GRANT signal. The gated clock line (output of the AND gates in Figure 4.3) which feeds the execution units are skewed a bit because of the delay through the latch and the AND gate. It affects the *precharge* phase but it has no affection on evaluate phase of the stage..

The control for clock-gating EUs is simple. The area and power overhead of the control unit circuitry are easily managed and sufficient power savings is achieved. If EU toggles between gated and non-gated modes, and on the same control circuitry keeps on switching which results in an increased overhead and the consumption of power in the control circuitry. To overcome *sequential priority policy* for execution units: In the EU of the same type, statically we can assign priorities to the units and set the priorities according to our requirement and desire[2].

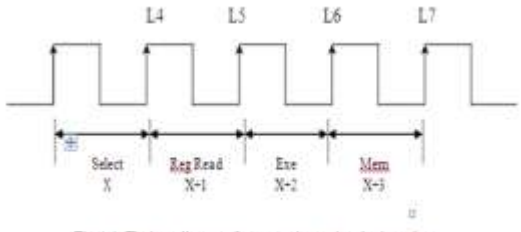

Fig 4.4. Timing diagram for execution units clock-gating.

4.2 Pipeline Latches

At the end of operation cycle (i.e. rename, register read, memory, execution and write back stage) the pipeline latches are clocked. The number of latches which should be clock-gated in any cycle should be known from the decode stage in prior cycle, for rename operation stage. the number of clock latches which should clock-gate in a cycle is defined by knowing it in the issue stage for any other stages of operation. In the issue stage "O" represents an empty issue slot and "1" represents a completely filled issue slot of issue instruction used in pipelining. In EU the clock is passed down by encoding in the pipe that is by extending the pipeline latches[15].

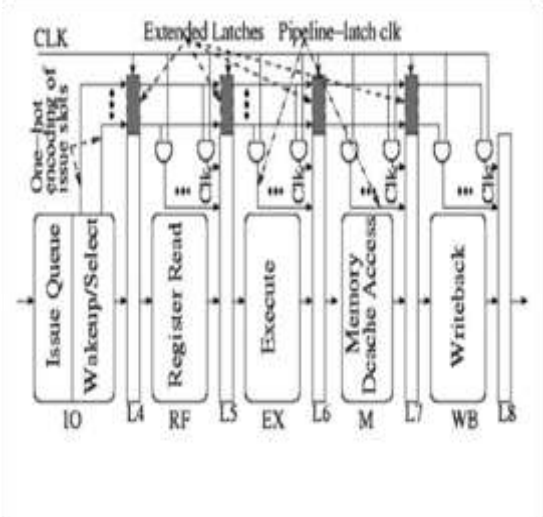

Figure 4.5. Clock-gating of pipeline latches.

Figure 4.5 depicts the clock-gating control for the stages which are following issue queue. The extended latches outputs which are suppose to carry the encoding are ANDed with the clock line which generates a number of gated clock inputs in pipelined latches.

The extensions to the pipeline latches and the extra AND gates for the control is small than that of the pipeline latches and clock drivers. Hence, the result of the extra control logic circuitry on area and power is not appreciable to an extent[15,2,20,23].

5. SIMULATION RESULTS OF GENERAL PURPOSE PROCESSOR

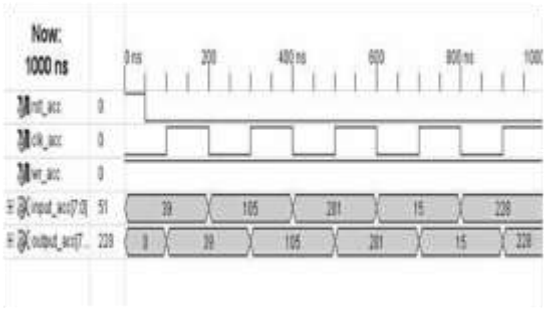

Figure 5.1: Accumulator output

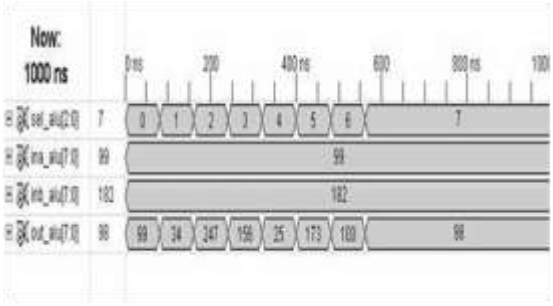

Figure 5.2: ALU output when the inputs are A = "01100011" and B = "10110110".

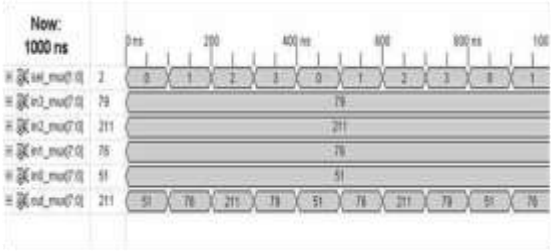

Figure 5.3: Multiplexer output.

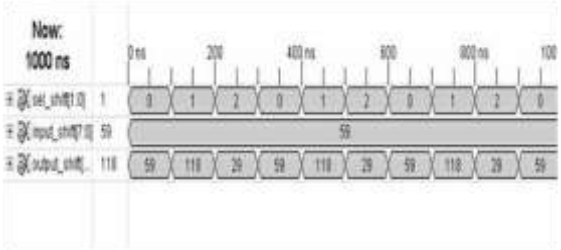

Figure 5.4: Regfile output.

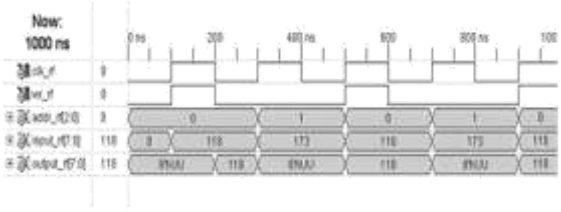

Figure 5.5: Shifter output when the input is "00111011".

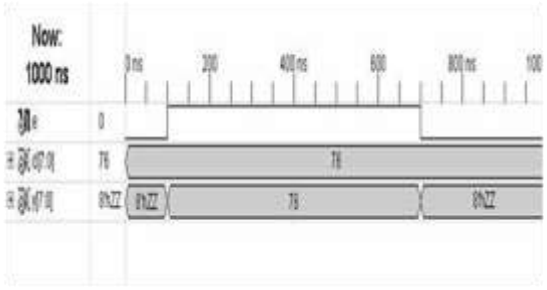

Figure 5.6: Tri-state buffer output.

VHDL is a hardware description language can be used to describe the behavior and structure of any digital systems. VHDL stands for VHSIC Hard ware Description Language, and VHSIC means very high speed integrated circuit. VHDL is used to describe and simulate the working and performance of a wide range of digital systems, ranging in various complexity from a few gates to an interconnection of many integrated circuits[2,10].

VHDL can categories a digital system at several different levels such as behavioral, dataflow and structural. VHDL leads by default use a top-down design approach, in which the system is initially specified at a high level and is tested using a simulator. After the system is error free at this level the design can gradually be improved eventually leading to structural description

6. CONCLUSION AND FUTURE WORK

In this Paper Implementation of Deterministic clock-gating technique has shown or many stages in modern pipeline architecture, a circuit block's whose usage in a specific cycle in the up-coming future is deterministically known a few cycles before time. Using this advance knowledge of information, Deterministic clock-gating clock-gates the execution units which are not used pipelined latches.

Results of Deterministic clock-gating are very efficient in reducing clock power. Power consumption is reduced upto20 – 35 % by this technique. As high-performance complex processor pipelines extends indefinitely and power becomes a more

important and concerned factor, Deterministic clock-gating effectiveness and simple design will overcome this indefinite extension in a pipelined architecture.

Effective clock-gating, however, requires a technique that determines which circuits are gated, when, and for how long. Intense care should be taken while designing the clock-gating control circuitry; otherwise the circuitry becomes overhead. This overhead results in power dissipation which is higher than that without clock-gating.

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